HUNG-MING CHEN

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EDUCATION

Ph.D. University of Texas at Austin — Aug 2003

M.S. University of Texas at Austin — Dec 1998

B.S. National Chiao Tung University, Hsinchu, Taiwan — June 1993

RESEARCH FOCUS

Design automation tools and methodologies for electronics

Automation on analog circuit and layout synthesis

2.5D/3D and heterogeneous integration methodologies

ML/DL based EDA optimization methodologies

PROFESSIONAL EXPERIENCE

Feb 2023–Jan 2026 Associate Dean, College of ECE, National Yang Ming Chiao Tung University, Taiwan

Aug 2021–present Senior Fellowship HEA (AdvanceHE, UK)

Aug 2018–July 2021 Director, Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan.

Jan 2015–Aug 2015 Visiting Professor, University of Illinois at Urbana-Champaign (UIUC), USA.

Aug 2012–present Professor, National Chiao Tung University, Hsinchu, Taiwan.

Jun 2010–Aug 2010 Visiting Professor, Synopsys, Hillsboro, OR, USA.

Sep 2008–Dec 2012 Visiting Research Professor, University of Kitakyushu, Japan.

Aug 2008–Jul 2012 Associate Professor, National Chiao Tung University, Hsinchu, Taiwan.

Aug 2003–Jul 2008 Assistant Professor, National Chiao Tung University, Hsinchu, Taiwan.

Jul 1995–Aug 1996 Assistant Engineer, Institute of Information Science, Academia Sinica, Taiwan.

TEACHING EXPERIENCE

NYCU 2003 – present

- Computer Programming: Basic C and C++ programming
- Discrete Mathematics: Basic math class in Computer Sciences (CS)
- Algorithms: Fundamental CS class
- EDA algorithms and implementation: Introductory EDA undergrad class
- Digital Circuits and Systems: Fundamental hardware design with Verilog
- VLSI Physical Design Automation: Graduate class in layout automation for IC
- Design for Manufacturability of VLSI: Graduate class for DFM
- Special topics on CAD: Graduate class for synthesis and verification for IC design
- Advanced Algorithms: Graduate class for algorithmic aspects in CS

UT-Austin 2000 – 2003

- Elements of Computers and Programming: Programming in Java

HONORS

- Second Prize, ACM/IEEE ICCAD CAD Contest "Power and Timing Optimization Using Multibit Flip-Flop" (with Ho et al.), 2024
- Third Prize, ACM/IEEE ICCAD CAD Contest "Power and Timing Optimization Using Multibit Flip-Flop" (with Chen et al.), 2024
- First Prize, ACM/IEEE ICCAD CAD Contest "Static IR Drop Estimation Using Machine Learning" (with Liu et al.), 2023
- Invited Talk at SASIMI, "ERI in Taiwan: How We Develop EDA Solutions for Reconfigurable Memory-Centric AI Edge Applications," 2021
- Fourth Place, ACM ISPD Clock-Aware FPGA Placement Contest (with Chen), 2017
- Fourth Place, ACM ISPD Routability-Driven FPGA Placement Contest (with Wu et al.), 2016
- First Prize, ACM Cadathlon (with Wang and Hu), 2014
- First Prize, ACM ISPD Detailed Routing-Driven Placement Contest (with Liu et al.), 2014
- Second Prize, ACM/IEEE ICCAD CAD Contest "Synopsys Platform Development" (with Huang et al.), 2014
- Second Prize, ACM/IEEE ICCAD CAD Contest "Incremental Timing Driven Placement" (with Wu et al.), 2014
- Second Prize, ACM Cadathlon (with Chin and Wang), 2012
- NCTU Excellent Teaching Awards, 2008 and 2009
- MOE SoC Consortium Outstanding Service Award, 2007

SERVICES

- IEEE Council on EDA Taipei Section Chair, 2016-2018
- IEEE Taipei Section Finance Officer, 2025-2027
- Taiwan Government Services
  - Program Director, National EDA Program for Heterogeneous Integration and Advanced Manufacturing, National Science and Technology Council, Taiwan, 2024-2029
  - Co-PI, Consortium of National Program on Intelligent Electronics, Ministry of Education, Taiwan, 2011-2014
  - Organizer, EDA Forum, DAT Consortium, Ministry of Education, Taiwan, 2004-2008
- Technical Program Committee (TPC) Member/Chair for
  - ACM/IEEE Design Automation Conference (DAC), 2024-present
  - IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2014-2016, 2020-present (2022-2025: track chair)
  - ACM International Symposium on Physical Design (ISPD), 2011-2013, 2022-2024
  - ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2007, 2009, 2014, 2018-present (2028 TPC Chair)
  - ACM Great Lakes Symposium on VLSI (GLSVLSI), 2018
  - IEEE SOC Conference (SOCC), 2006-2020
  - IEEE VLSI-DAT, 2009-2018 (2015-2018: EDA track co-chair)
  - IEEE International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), 2019-present
  - IEEE/ACM International Workshop on System-Level Interconnect Prediction (SLIP), 2018-2021
  - VLSI Design/CAD Symposium, Taiwan, 2004-present
  - CAD Contest, Ministry of Education Taiwan and IEEE CEDA, 2003-present
  - Synthesis And System Integration of Mixed Information technologies (SASIMI Japan), 2009-present (2019 TPC Chair)
- Organizing Committee (OC) Member/Chair for
  - ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC) 2010 and 2022
  - IEEE VLSI-DAT 2021 (Special Session Organizer)
  - Synthesis And System Integration of Mixed Information technologies (SASIMI) 2010 and 2015 (2024 General Chair)
  - VLSI Design/CAD Symposium, Taiwan, 2008 and 2017
  - International Conference on Field-Programmable Technology (ICFPT) 2008
  - IEEE SOC Conference (SOCC) 2007
  - IEEE International Workshop on Memory Technology, Design, and Testing (MTDT) 2007

GOVERNMENT FUNDED RESEARCH PROJECTS

- "High Performance Neuromorphic Computing System," May 2021–Oct 2025, National Science and Technology Council (NSTC) 4.5 year Integrated Research Project
- "Design and Technology Co-Optimization Assisted AMS Layout Synthesis," Aug 2022–July 2025, National Science and Technology Council (NSTC) 3-year Project
- "EDA solutions for memory-centric AI edge: system evaluation and implementation for reconfigurability," Nov 2019–Oct 2022, Ministry Of Science and Technology (MOST) 3-year Taiwan-ERI Project
- "Machine and Deep Learning Based Circuit and Layout Synthesis for Digital and Analog Designs," Aug 2019–Jul 2022, Ministry Of Science and Technology (MOST) 3-Year Project
- "Routing in Cyberphysical Active-Matrix Based Digital Microfluidic Biochips," Aug 2017–Jul 2019, Ministry Of Science and Technology (MOST) 2-Year Project
- "Advanced Low Voltage High-Speed Low-Power Memory Design," Aug 2017–Jul 2019, MOST Industrial-Academic Technology Consortium Integrated Research Project
- "Ambient Analytics in Intelligent Manufacturing–Main Project and Subproject 3: Analog Layout Prototyping via Deep Learning," Aug 2016–Jul 2019, MOST Integrated Research Project
- "Data Analytics Based Electronic Design Automation–Subproject 2: Datapath Identification and Placement via Customized Clustering and Learning," May 2014–Apr 2016, MOST Integrated Research Project
- "Electronic Design Automation for Large Scale Microfluidic Biochip –Subproject 2: The Study of Fluid Routing Automation and Design Integration for Microfluidic Biochip," May 2014–Apr 2016, MOST Integrated Research Project
- "Parallel and Distributed Electronic Design Automation–Main Project and Subproject 2: Parallel and Distributed Algorithms in Mixed-Size Placement Optimization," May 2011–Jul 2014, National Science Council (NSC) Integrated Research Project
- "Electronic Design Automation for 3D Integration–Main Project and Subproject 4: 3D-SIC and 3D-SIP Design Planning," Aug 2009–Jul 2011, NSC Integration Project
- "A Novel Methodology in Chip-Package-Board Co-design and Co-optimization," Aug 2008–Jul 2011, NSC 3-Year Research Project
- "On Increasing Design Reliability in Advanced Manufacturing Technology–Main Project and Subproject 3: Yield Improvement Methodologies in Post-Layout Design Flow and Design for Test," Aug 2006–Jul 2009, NSC Integrated Research Project
- "Core Technology for e-Home Environment–Subproject 6: Power Supply Planning and Noise Avoidance in SoC Floorplan Design," Aug 2004–Jul 2007, NSC Integrated Research Project
- "System-on-Chip IP Collections and Verification," Apr 2004–Mar 2007, Ministry of Economic Affairs (MOEA) Integrated Research Project
- "Design and Automation for Low-Power Systems–Subproject 7: Floorplanning with Aggressive Power Optimization," Nov 2003–Jul 2006, NSC Integrated Research Project

INDUSTRY FUNDED PROJECTS

- "Standard Cell Layout Generation and Optimization in Nanosheet Technology with OD Jog and SPR Consideration," July 2025–June 2027, funded by MediaTek (MTK), Hsinchu, Taiwan
- "System and Chip Level Power Network Optimization and Crosstalk Prediction on Fanout Packages," Jan 2017–present, funded by EOSL, Industrial Technology Research Institute of Taiwan (ITRI)
- "Design Planning and Synthesis for 3D Integration," May 2024–April 2025, funded by Cadence
- "Power Integrity and InFO Optimization for 2.5D/3DICs," May 2019–2024, funded by TSMC, Taiwan
- "Advanced Node Cell Library Migration," May 2021–Apr 2022, funded by NovaTek, Hsinchu, Taiwan
- "Routability Improvement on DDIC APR," Feb 2020–Jan 2021, funded by NovaTek, Hsinchu, Taiwan
- "Timing Driven Partition for Multi-FPGA Architecture," Dec 2019–Nov 2021, funded by Synopsys
- "Low Voltage High-Speed SRAM System Design," Mar 2017–Jul 2019, funded by Etron, Taiwan
- "Advanced Node Custom Layout Synthesis," Jun 2015–May 2016, funded by TSMC, Taiwan
- "Thermal and Stress Migration Study for Microbump Interconnect in BGA Package," Sep 2012–Aug 2014, funded by SPIL (ASE Holdings), Taiwan
- "3D IC Power Network Modeling and Synthesis," 2011–2016, funded by ICRL, Industrial Technology Research Institute of Taiwan (ITRI)
- "LDO Design and Automation," Feb 2008–Jan 2009, funded by MediaTek (MTK), Hsinchu, Taiwan

PUBLICATIONS

Books and Book Chapters

B3 K.-N. Tu, C. Chen and H.-M. Chen, "Electronic Packaging Science and Technology, " Wiley, 2022

B2 K.-C. Wang and H.-M. Chen, "Multilevel Large-Scale Modules Floorplanning/Placement with Improved Neighborhood Exchange in Simulated Annealing," in *Simulated Annealing, Theory with Applications*, Sciyo, 2010

B1 H.-M. Chen, D.F. Wong, H. Zhou, F.Y. Young, H.H. Yang, and N. Sherwani, "Integrated Floorplanning and Interconnect Planning," in *Layout Optimization in VLSI Designs*, Kluwer Academic Publishers, 2001

ACM/IEEE Journal Papers

J26 C.-A. Yu, Y.-T. Liu, Y.-H. Cheng, S.-Y. Wu, H.-M. Chen, C.-C. Jay Kuo, "GIRD: A Green IR-Drop Estimation Method," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), Early Access

J25 Thasreefa AK, A. Patyal, H.-Y. Chi, Mark P.-H. Lin and H.-M. Chen, "On Reducing LDE Variations in Modern Analog Placement," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD) 42(4). April 2023

J24 A. Patyal, H.-M. Chen, Mark P.-H. Lin, G.-Q. Fang, Simon Y.-H. Chen, "Pole-aware Analog Layout Synthesis Considering Monotonic Current Flows and Wire-Crossings," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD) 42(1), January 2023

J23 W. Lu, P.-T. Huang, H.-M. Chen, and W. Hwang, "An Energy-Efficient 3D Cross-Ring Accelerator with 3D-SRAM Cubes for Hybrid Deep Neural Networks," IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS) 11(4), December 2021

J22 Asha K. A., L.-E. Hsu, A. Patyal, and H.-M. Chen, "Improving the Quality of RO-PUF by Principal Component Analysis (PCA)," *ACM Journal on Emerging Technologies in Computing*(JETC), 17(3), June 2021, Article 34

J21 H.-Y. Chi, Z.-J. Lin, C.-H. Hung, C.-N. Liu, and H.-M. Chen, "A Style-based Analog Layout Migration Technique with Complete Routing Behavior Preservation," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), 40(12), December 2020

J20 A. Patyal, P.-C. Pan, Asha K A, H.-M. Chen and W.-Z. Chen, "Exploring Multiple Analog Placements with Partial-Monotonic Current Paths and Symmetry Constraints using PCP-SP," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), 39(12), February 2020

J19 H.-Y. Chi, C.-N. Liu, and H.-M. Chen, "Wire Load Oriented Analog Routing with Matching Constraints," *ACM Transactions on Design Automation of Electronics Systems* (TODAES), 25(6), October 2020, Article 55

J18 G.-R. Lu, A. Banerjee, B. B. Bhattacharya, T.-Y. Ho, and H.-M. Chen, "Reliability Hardening Mechanisms in Cyber-Physical Digital-Microfluidic Biochips," *ACM Journal on Emerging Technologies in Computing*(JETC), 14(3), October 2018, Article 34

J17 G.-R. Lu, C.-H. Kuo, K.-C. Chiang, A. Banerjee, B. B. Bhattacharya, T.-Y. Ho, and H.-M. Chen, "Flexible Droplet Routing in Active-Matrix Based Digital Microfluidic Biochips," *ACM Transactions on Design Automation of Electronic Systems* (TODAES), 23(3), April 2018, Article 37

J16 P.-C. Pan, C.-Y. Chin, H.-M. Chen, T.-C. Chen, C.-C. Lee, and J.-C. Lin, "A Fast Prototyping Framework for Analog Layout Migration with Planar Preservation," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), 34(9), September 2015

J15 C.-K. Wang, Y.-C. Chang, H.-M. Chen, C.-Y. Chin, "Clock Tree Synthesis Considering Slew Effect on Supply Voltage Variation," *ACM Transactions on Design Automation of Electronics Systems* (TODAES), 20(1), November 2014, Article 3

J14 S.-Y. Liu, C.-H. Chang, H.-M. Chen and T.-Y. Ho, "ACER: An Agglomerative Clustering Based Electrode Addressing and Routing Algorithm for Pin-Constrained EWOD Chips," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), 33(9), September 2014

J13 S.-Y. Liu, R.-G. Luo, S. Aroonsantidecha, C.-Y. Chin, and H.-M. Chen, "A Fast Thermal Aware Placement with Accurate Thermal Analysis Based on Green Function," *IEEE Transactions on Very Large Scale Integration Systems* (TVLSI), 22(6), June 2014

J12 R.-J. Lee, H.-W. Hsu and H.-M. Chen, "Board- and Chip-Aware Package Wire Planning," *IEEE Transactions on Very Large Scale Integration Systems* (TVLSI), 21(8), August 2013

J11 S.-Y. Liu, W.-T. Lo, C.-J. Lee, and H.-M. Chen, "Agglomerative- Based Flip-Flop Merging and Relocation for Signal Wirelength and Clock Tree Optimization," *ACM Transactions on Design Automation of Electronic Systems* (TODAES), 18(3), July 2013, Article 40

J10 C.-Y. Chin, C.-Y. Kuan, T.-Y. Tsai, H.-M. Chen and Y. Kajitani, "Escaped Boundary Pins Routing for High Speed Boards, " *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), 32(3), March 2013

J09 R.-J. Lee and H.-M. Chen, "A Study of Row-Based Area-Array I/O Design Planning in Concurrent Chip-Package Design Flow," *ACM Transactions on Design Automation of Electronic Systems* (TODAES), 18(2), March 2013, Article 30

J08 R.-J. Lee and H.-M. Chen, "Efficient Package Pin-Out Planning with System Interconnects Optimization for Package-Board Codesign," *IEEE Transactions on Very Large Scale Integration Systems* (TVLSI), 19(5), May 2011

J07 C.-Y. Lin, H.-C. Lin, and H.-M. Chen, "On Reducing Test Power and Test Volume by Effective Pattern Compression Schemes," *IEEE Transactions on Very Large Scale Integration Systems* (TVLSI), 18(8), pp.1220-1224, August 2010

J06 M.-C. Wu, M.-C. Lu, H.-M. Chen, and J.-Y. Jou, "Performance-Constrained Voltage Assignment in Multiple Supply Voltage SoC Floorplanning," *ACM Transactions on Design Automation of Electronic Systems* (TODAES), 15(1), December 2009, Article 3

J05 R.-J. Lee and H.-M. Chen, "Fast Flip-Chip Pin-Out Designation Respin for Package-Board Codesign," *IEEE Transactions on Very Large Scale Integration Systems* (TVLSI), 17(8), pp.1087-1098, August 2009

J04 C.-H. Lu, H.-M. Chen, and C.-N. Liu, "Effective Decap Insertion in Area-Array SoC Floorplan Design," *ACM Transactions on Design Automation of Electronic Systems* (TODAES), 13(4), September 2008, Article 66

J03 C.-Y. Chang and H.-M. Chen, "Design Migration from Peripheral ASIC Design to Area-IO Flip-Chip Design by Chip I/O Planning and Legalization," *IEEE Transactions on Very Large Scale Integration Systems* (TVLSI), 16(1), pp. 108-112, January 2008

J02 H.-M. Chen, I-Min Liu, and D.F. Wong, "I/O Clustering in Design Cost and Performance Optimization for Flip-Chip Design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), 25(11), pp. 2552-2556, November 2006

J01 H.-M. Chen, L.-D. Huang, I-Min Liu, and D.F. Wong, "Simultaneous Power Supply Planning and Noise Avoidance in Floorplan Design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), 24(4), pp. 578-587, April 2005

Other Journal Papers

O09 J.-D. Li, C.-H. Kuo, G.-R. Lu, S.-J. Wang, Katherine S.-M. Li, T.-Y. Ho, H.-M. Chen and S. Hu, "Co-placement Optimization in Sensor-reusable Cyber-physical Digital Microfluidic Biochips, " *Microelectronics Journal* 83, pp. 185-196, January, 2019

O08 C.-H. Lu, H.-M. Chen, C.-N. Liu and W.-Y. Shih, "Package Routability and IR-Drop-Aware Finger/Pad Planning for Single Chip and Stacking IC Designs," *Integration, the VLSI Journal*, May 2012

O07 C.-Y. Lin and H.-M. Chen, "A Generic Multi-Dimensional Scan-Control Scheme for Test-Cost," *Journal of Information Science and Engineering* (JISE), November 2011

O06 C.-H. Lu, H.-M. Chen, and C.-N. Liu, "Design Planning with 3D-Via Optimization in Alternative Stacking Integrated Circuits," *Journal of Information Science and Engineering* (JISE), January 2011

O05 C.-Y. Lin, L.-C. Hsu, and H.-M. Chen, "On Reducing Test Power, Volume and Routing Cost by Chain Reordering and Test Compression Techniques," *IEICE Transactions on Electronics*, vol. E93-C no. 3, pp.369-378, March 2010

O04 C.-Y. Lin, H.-C. Lin, and H.-M. Chen, "A Methodology with Selective Pattern Compression Schemes on Reducing Test Power and Test Volume," *International Journal of Electrical Engineering* (IJEE), 17(1), pp. 75-88, January 2010

O03 Y.-C. Lin, H.-A. Chien, C.-C. Shih, and H.-M. Chen, "A Multi-layer Obstacles-Avoiding Router Using X-Architecture," *WSEAS Transaction on Circuits and Systems*, Issue 8, Volume 7, August 2008

O02 Bruce Tseng and H.-M. Chen, "Dual-Vdd Voltage Island-Aware Buffered Routing Tree Construction," *International Journal of Electrical Engineering* (IJEE), 15(2), pp.117-126, April 2008

O01 C.-H. Lu, H.-M. Chen, and C.-N. Liu, "An Effective Decap Insertion Method Considering Power Supply Noise During Floorplanning," *Journal of Information Science and Engineering* (JISE), 24(1), pp.115-127, January 2008

ACM/IEEE Conference/Workshop Papers

C122 C.-Y. Hsieh, H.-M. Chen, S.-H. Wu, C.-M. Hsu and W.-H Liu, "On Efficient Crosstalk Predictability for Fanout Package Designs," *Proc. of IEEE International System on Chip Conference*, September 2025 (SOCC-25)

C121 C.-Y. Chiang et al., "Late Breaking Results: Scalable GPU-Friendly Parallelization for Sweep-Based Maze Routing," *Proc. of ACM/IEEE Design Automation Conference*, June 2025 (DAC-25)

C120 S.-S. Lin, S.-Y. Chen, Y.-P. Huang, T.-C. Lin, H.-M. Chen and W.-Z. Chen, "Clock and Power Supply-Aware High Accuracy Phase Interpolator Layout Synthesis," *Proc. of IEEE/ACM Design, Automation and Test in Europe*, March 2025 (DATE-25)

C119 H.-J. Chang, Y.-H. Chen, H.-W. Huang, Y.-H. Yeh, H.-M. Chen and C.-N. Jimmy Liu," On Awareness of Offset-Via and Teardrop in Advanced Packaging Interconnect Synthesis," *Proc. of ACM/IEEE Asia and South Pacific Design Automation conference*, January 2025 (ASP-DAC-25)

C118 C.-Y. Chiang et al., "Mixed-Size Placement Prototyping Based on Reinforcement Learning with Semi-Concurrent Optimization," *Proc. of ACM/IEEE Asia and South Pacific Design Automation conference*, January 2025 (ASP-DAC-25)

C117 Y.-T. Liu, Y.-H. Cheng, S.-Y. Wu and H.-M. Chen," CFIRSTNET: Comprehensive Features for Static IR Drop Estimation with Neural Network," *Proc. of IEEE/ACM International Conference on Computer-Aided Design*, November 2024 (ICCAD-24)

C116 B.-H. Li, K.-C. Lin, H. Zuo, P.-C. Pan, H.-M. Chen, S.-J. Jou, C.-N. Jimmy Liu and B.-C. Lai, " Efficient Analog Layout Generation for In-RRAM Computing Circuits via Area and Wire Optimization," *Proc. of IEEE International Midwest Symposium on Circuits and Systems Conference*, August 2024 (MWSCAS-24)

C115 S.-H. Chang, S.-Y. Chen, C.-W. Yang, H.-W. Huang, Y.-C. Yang, W.-L. Chen, C.-N. Jimmy Liu and H.-M. Chen, " Mitigating Power and Process Variation for Analog CIM Design Migration, " *Proc. of International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design*, July 2024 (SMACD-24)

C114 W. Lu et al., "Scalable Embedded Multi-Die Active Bridge (S-EMAB) Chips with Integrated LDOs for Low-Cost Programmable 2.5D/3.5D Packaging Technology," *Proc. of IEEE Symposium on VLSI Technology and Circuits*, June 2024 (VLSI-Tech-24)

C113 B.-J. Shih et al., "3DIC with Stacked FinFET, Inter-Level Metal, and Field-Size (2533mm2) Single-Crystalline Si on SiO2 by Elevated-Epi," *Proc. of IEEE Symposium on VLSI Technology and Circuits*, June 2024 (VLSI-Tech-24)

C112 B.-K. Kang, H.-J. Chang, H.-M. Chen and C.-N. Jimmy Liu,"ML/DL-Based Signal Integrity Optimization for InFO Routing," *Proc. of IEEE International NEWCAS Conference*, June 2024 (NEWCAS-24)

C111 W. Lu, H.-H. Pei, J.-R. Yu, H.-M. Chen and P.-T. Huang, "A 28nm Energy-Area-Efficient Row-based pipelined Training Accelerator with Mixed FXP4/FP16 for On-Device Transfer Learning,"*Proc. of IEEE International Symposium on Circuits and Systems*, May 2024 (ISCAS-24)

C110 C.-C. Lin, W. Lu, P.-T. Huang and H.-M. Chen, "A 28nm 343.5fps/W Vision Transformer Accelerator with Integer-Only Quantized Attention Block," *Proc. of IEEE International Conference on AI Circuits and Systems*, July 2023 (AICAS-24)

C109 H.-M. Chen, "Enabling System Design in 3D Integration: Technologies and Methodologies," *Proc. of ACM International Symposium on Physical Design*, March 2024 (ISPD-24) **(invited)**

C108 P.-C. Wang, P.-H. Lin, C.-N. Liu and H.-M. Chen, "Layout Synthesis of Analog Primitive Cells with Variational Autoencoder," *Proc. of International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design*, July 2023 (SMACD-23)

C107 Asha K. A., A. Patyal and H.-M. Chen, "On Reliability Hardening of FPGA based RO-PUF by using Regression Methodologies," *Proc. of IEEE International Symposium on VLSI Technology, Systems and Applications*, April 2023 (VLSI-TSA-23)

C106 H.-M. Chen, C.-L. Hsiao, W.-T. Chao and I-C. Hsieh, "On Generating Cell Library in Advanced Nodes: Efforts and Challenges," *Proc. of IEEE International Symposium on VLSI Technology, Systems and Applications*, April 2023 (VLSI-TSA-23) **(Invited)**

C105 P.-Y. Chen, C.-Y. Liu, H.-M. Chen and P.-T. Huang, "On-Interposer Decoupling Capacitors Placement for Interposer-based 3DIC," *Proc. of IEEE International Symposium on Quality of Electronic Design*, April 2023 (ISQED-23)

C104 H.-M. Chen, C.-W. Ho, S.-H. Wu, W. Lu, P.-T. Huang, H.-J. Chang and C.-N. Liu, "Reshaping System Design in 3D Integration: Perspectives and Challenges," *Proc. of ACM International Symposium on Physical Design*, March 2023 (ISPD-23) **(invited)**

C103 C.-Y. Chiang, C.-L. Hu, P.-H. Lin, Y.-S. Chung, S.-J. Jou, J.-T. Wu, S.-H. Chiang, C.-N. Liu and H.-M. Chen, "On Automating Finger-Cap Array Synthesis with Optimal Parasitic Matching for Custom SAR ADC, " *Proc. of ACM/IEEE Asia and South Pacific Design Automation conference*, January 2023 (ASP-DAC-23)

C102 Y.-H. Yeh, Y.-H. Chen, H.-M. Chen, D.-Y. Tu, G.-Q. Fang, Y.-C. Kuo, P.-Y. Chen, " DPRoute: Deep Learning Framework for Package Routing, " *Proc. of ACM/IEEE Asia and South Pacific Design Automation conference*, January 2023 (ASP-DAC-23)

C101 C.-Y. Chiang, C.-L. Hu, Mark P.-H. Lin, K.-Y. Chang, S.-J. Jou, H.-Y. Chen, C.-N. Liu and Hung-Ming Chen, "On Optimizing Capacitor Array Design for Advanced Node SAR ADC," *Proc. of International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design*, July 2022 (SMACD-22)

C100 J. Zhang, W. Lu, P.-T. Huang, S.-H. Li, T.-Y. Hung, S.-H. Wu, M.-J. Dai, I-S. Chung, W.-C. Chen, C.-H. Wang, S.-S. Sheu, H.-M. Chen, K.-N. Chen, W.-C. Lo, C.-I Wu, "An Embedded Multi-Die Active Bridge (EMAB) Chip for Rapid-Prototype Programmable 2.5D/3D Packaging Technology," *Proc. of IEEE Symposium on VLSI Technology and Circuits*, June 2022 (VLSI-Tech-22)

C99 Y.-H. Yeh, Simon Y.-H. Chen, H.-M. Chen, D.-Y. Tu, G.-Q. Fang, Y.-C. Kuo and P.-Y. Chen, "Substrate Signal Routing Solution Exploration for High-Density Packages with Machine Learning, " *Proc. of IEEE International Symposium on VLSI Design, Automation, and Test*, April 2022 (VLSI-DAT-22) **(Invited)**

C98 H.-Y. Chi, Simon Y.-H. Chen, H.-M. Chen, C.-N. Liu, Y.-C. Kuo, Y.-H. Chang and K.-H. Ho, "Practical Substrate Design Considering Symmetrical and Shielding Routes," *Proc. of IEEE/ACM Design, Automation and Test in Europe*, March 2022 (DATE-22)

C97 B.-C. Lai, T.-C. Chiang, P.-S. Kuo, W.-C. Wang, Y.-L. Hung, H.-M. Chen, C.-N. Liu and S.-J. Jou, "DASC : A DRAM Data Mapping Methodology for Sparse Convolutional Neural Networks", *Proc. of IEEE/ACM Design, Automation and Test in Europe*, March 2022 (DATE-22)

C96 H. M. Chen et al., On Reconfiguring Memory-Centric AI Edge Devices for CIM, IEEE ISOCC, October 2021 **(Invited)**

C95 Y.-Y. Huang, C.-T. Lin, W.-L. Liang and H.-M. Chen, "Learning Based Placement Refinement to Reduce DRC Short Violations, " *Proc. of IEEE International Symposium on VLSI Design, Automation, and Test*, April 2021 (VLSI-DAT-21)

C94 H.-M. Chen et al., "On EDA Solutions for Reconfigurable Memory-Centric AI Edge Applications," *Proc. of IEEE/ACM International Conference on Computer-Aided Design*, November 2020 (ICCAD-20) **(Invited)**

C93 P.-H. Lin, H.-Y. Chi, A. Patyal, Z.-Y. Liu, J.-J. Zhao, C.-N. Liu and H.-M. Chen, "Achieving Analog Layout Integrity through Learning and Migration," *Proc. of IEEE/ACM International Conference on Computer-Aided Design*, November 2020 (ICCAD-20) **(Invited)**

C92 P.-T. Huang, T.-H. Tsai, P.-J. Yang, W. Hwang and H.-M. Chen, "Hierarchical Active Voltage Regulation for Heterogeneous TSV 3D-ICs," *Proc. of IEEE International System on Chip Conference*, September 2020 (SOCC-20)

C91 A. Patyal, H.-M. Chen and P.-H. Lin, "Pole-aware Analog Placement Considering Monotonic Current Flow and Crossing-Wire Minimization (LBR)," *Proc. of ACM/IEEE Design Automation Conference*, July 2020 (DAC-20)

C90 M.-Y. Huang and H.-M. Chen et al., "A Design Flow for Micro Bump and Stripe Planning on Modern Chip-Package Co-Design," *Proc. of IEEE Electronic Components and Technology Conference*, May 2020 (ECTC-20)

C89 H.-Y. Chang, H.-M. Chen, Y.-C. Kuo, H.-T. Tsai, Simon Y.-H. Chen, J.-R. Jiang, and Y.-Y. Chien, "Irregular Bumps Design Planning for Modern Ball Grid Array Packages," *Proc. of IEEE Electronic Components and Technology Conference*, May 2020 (ECTC-20)

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C32 C.-Y. Lin and H.-M. Chen, "A Novel Two-Dimensional Scan-Control Scheme for Test-Cost Reduction," *Proc. of IEEE International Symposium on Quality of Electronic Design*, March 2010 (ISQED-10)

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APPENDIX: RESEARCH SUMMARY

1. Chip-package-board co-design and 2.5D/3D IC :

- We have greatly improved existing cell placement by I/O clustering and legalization, considering design cost reduction and signal integrity preservation. (ICCD-04, VLSI-DAT-06, TCAD-Nov-06, TVLSI-Jan-08)
- We have proposed some approaches to implementing important issues for chip-package and package-board codesign. (ASP-DAC-07, ISQED-08, DATE-09, TVLSI-Aug-09, TVLSI-May-10, ASP-DAC-14)
- We have developed a framework for automatic board-level routing for package-board coplanning, and implemented an approach to RDL routing using pseudo single RDL layer concept (used in design service company). (DATE-11, DATE-12)
- We have proposed a standard cell placement by min-cut partitioning for one layer after layer assignment and addressed alignment and timing constraint considering TSV models. (DATE 3D Integration Workshop-11, SOCC-11)
- Design flows and RDL routing for 2.5D/3D integration are developed. (DATE-20, ECTC-20 VLSI-22, VLSI-DAT-22, DATE-22)
- We are invited to give perspectives on 3D integration. (ISPD-23, ISPD-24)

2. Analog design automation and layout synthesis :

- We have presented a synthesis framework for nanometer analog, mixed-signal, and radio-frequency circuit design, has both the advantages of accuracy and efficiency, accomplished by integrating both circuit simulator and analytic formulation. (ISQED-11, DAC-19)
- We have proposed fast prototyping methods for layout migration of nanometer designs. They show analog layout migration methodologies to quickly provide multiple layouts while keeping similar or better circuit performance. (ICCAD-11, ICCAD-12, ICCAD-13, ICCAD-20, TCAD-Sep-15, SMACD-18 and 19)
- We have reinvented sequence pair for current path constraints in analog layout synthesis. (DAC-18, DAC-20, TCAD-Dec-20)
- We have proposed a novel template-based analog layout synthesis methodology for phase interpolator. (DATE-25)

3. Power delivery network synthesis and power-aware designs :

- We have developed methodologies for signal integrity issues, including decoupling capacitors (decap) insertion during floorplanning and power delivery compensation by low level metal lines. (ASP-DAC-07, TODAES-Sep-08)
- We have developed new and practical methodologies for power network prototyping, including 3D stacking memory model. (DATE-13, ICCD-14, ASP-DAC-17, ISCAS-19)
- By modeling to association rule mining, we can achieve an optimal solution for noise sensor placement with the number of sensors used less than half of the number from the state-of-the-art.(GLSVLSI-16)
- We have proposed an approach to simultaneously minimizing power and routing cost in scan chain reordering after cell placement. (ISQED-06) Furthermore, we have also proposed a novel architecture for test power and volume reduction. (ICCAD-07, TVLSI-Aug-10)
- We have developed methodologies which can be applied in buffered clock tree construction to achieve low short-circuit power. (SOCC-06)
- We have implemented several approaches regarding some recent low power techniques (such as voltage islands, power gating, multiple supply voltage (MSV), and multi-bit flip-flop (MBFF)) to reduce the power consumption and to plan the clock of the chip. (SOCC-06, ISPD-08, SOCC-07, ISQED-11, DATE-12)

4. **Machine learning-powered circuit and package layout synthesis** :

   - We provided learning-based methodologies on circuit/layout synthesis and DRV reduction of VLSI designs. (VLSI-DAT-18, VLSI-DAT-21, DAC-19, ICCAD-20)
   - Learning-based methodology on package layout is provided. (NEWCAS-24)
   - DL-based IR-drop prediction framework is developed, and it is also the winner of CAD contest 2023. (ICCAD-24)
   - We have developed DL-based crosstalk predition for fanout packages. (SOCC-25)

5. **VLSI and FPGA routability-driven placement** :

   - We have developed a state-of-the-art placer and won the first prize of ACM ISPD detailed routing driven placement contest in 2014. (ISPD-15)
   - We have continued to develop FPGA analytical placer using rough placed packing in 2017. (VLSI-DAT-17)

6. **EDA solutions for analog compute-in-memory** :

   - We proposed memory-centric design architectures, analog-based IMC and EDA solutions (from system reconfiguration to layout optimization). (ICCAD-20, ISOCC-21, SMACD-20)
   - We have developed efficient layout generation for In-RRAM computing circuits. (MWSCAS-24)

7. **Chip design security** :

   - We provided solutions in improving the quality and the reliability of physically unclonable function design in FPGA. (AsianHOST-18, JETC-Jun-21)

8. **Digital microfluidic biochip (DMFB) design automation** :

   - We provided a routability estimation algorithm to solve pin-count aware problem on DMFBs. Our algorithm can also realize on biochips with obstacles and control the total number of pin reduction (TCAD-Sep-14). Related emerging routing and reliability concerns are investigated (JETC-18 and TODAES-Apr-18).
   - We proposed the first module and sensor co-placement algorithm which can effectively satisfy the sensor constraint and the reliability of electrodes in cyber-physical DMFBs. (BioCAS-16)

9. **Design for manufacturability and reliability** :

   - We have proposed an approach to minimizing the topography variation in multi-layer oxide and Copper CMP manufacturability. (VLSI-DAT-08)
   - We have developed a framework for efficient and optimal redundant via insertion based on network flow algorithm. (GLSVLSI-08)
   - We started to work on electro-static discharge (ESD) protection, and I/O-clamp coplacement for flip-chip designs. (ICCAD-14)