



VLSI Design Automation Lab

超大型積體電路(實體)設計自動化實驗室

Prof. Hung-Ming Chen 陳宏明教授

Institute of Electronics, NYCU, Taiwan

hmchen@nycu.edu.tw

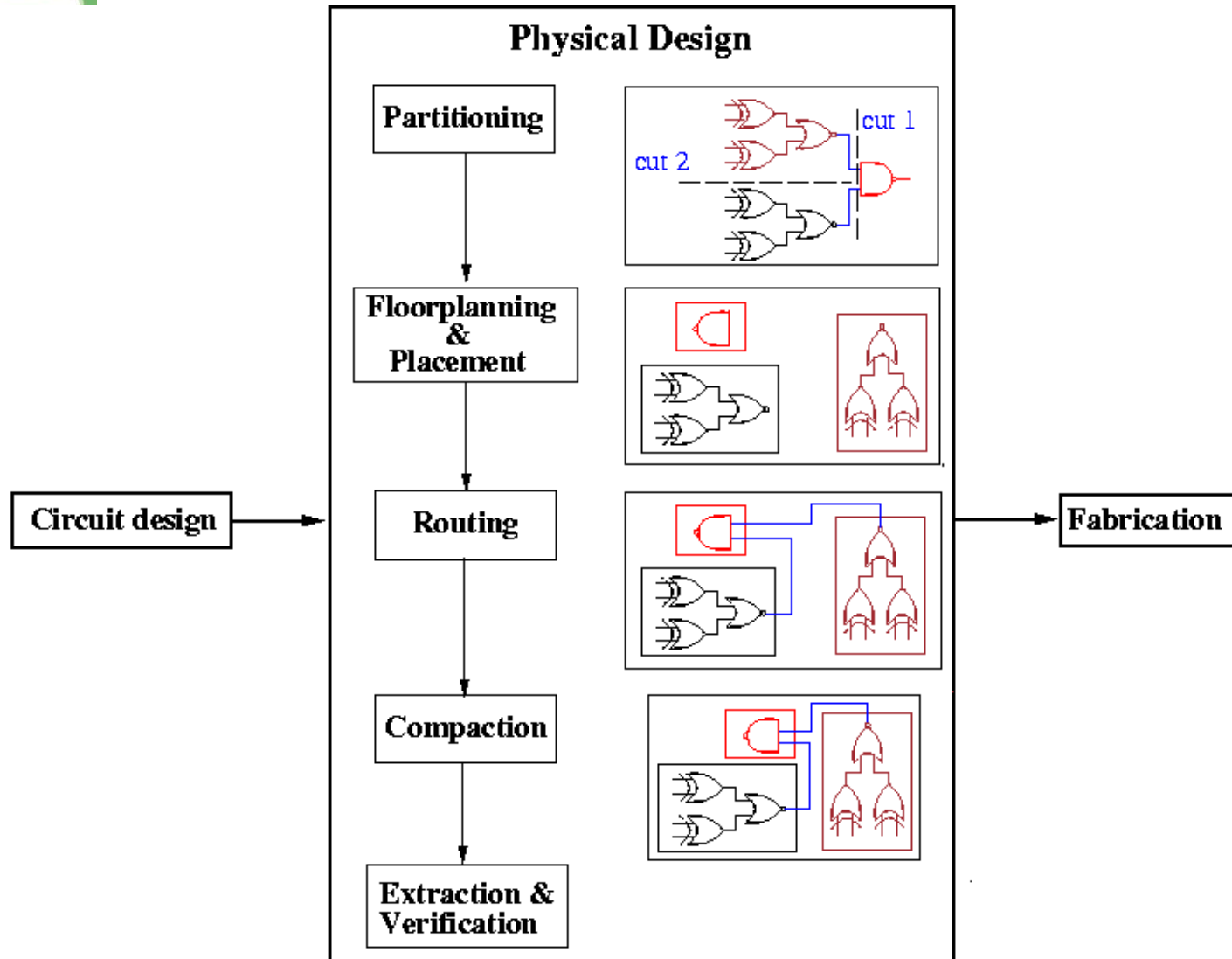


About Advisor



- Intel internship, 1999
- Ph.D. @ UTCS, joined NCTU EE, 2003
- Visiting Research Professor
 - University of Kitakyushu, Japan, 2008-2012
 - Synopsys, Hillsboro, OR, USA, 2010
 - University of Illinois at Urbana-Champaign (UIUC), USA, 2015
- TPC members in DAC, ICCAD, ISPD, ASPDAC, DATE
- Director, Institute of Electronics, 2018-2021
- Associate Dean, ECE College, 2024-2026

Physical Design Flow



國際賽得獎榮譽 2012-2017

- Fourth Place, ACM ISPD FPGA Placement Contest, 2016 and 2017
- First Prize, ACM CADathlon (with Wang and Hu), 2014
- First Prize, ACM ISPD “Detailed Routing-Driven Placement Contest” (with S. Liu et al.), 2014
- Second Prize, ACM/IEEE ICCAD CAD Contest “Synopsys Platform Development” (with Huang et al.), 2014
- Second Prize, ACM/IEEE ICCAD CAD Contest “Incremental Timing Driven Placement” (with W.-C. Wu et al.), 2014
- Second Prize, ACM CADathlon (with Chin and Wang), 2012



Welcome to the CADathlon @ ICCAD

Congratulations to the 2012 Winners

First Place: Hung-Chih Ou and Po-Ya Hsu (National Taiwan University); Advisor: Yao-Wen Chang

Second Place: Ching-Yu Chin and Chun-Kai Wang (National Chiao Tung University); Advisor: Hung-Ming Chen

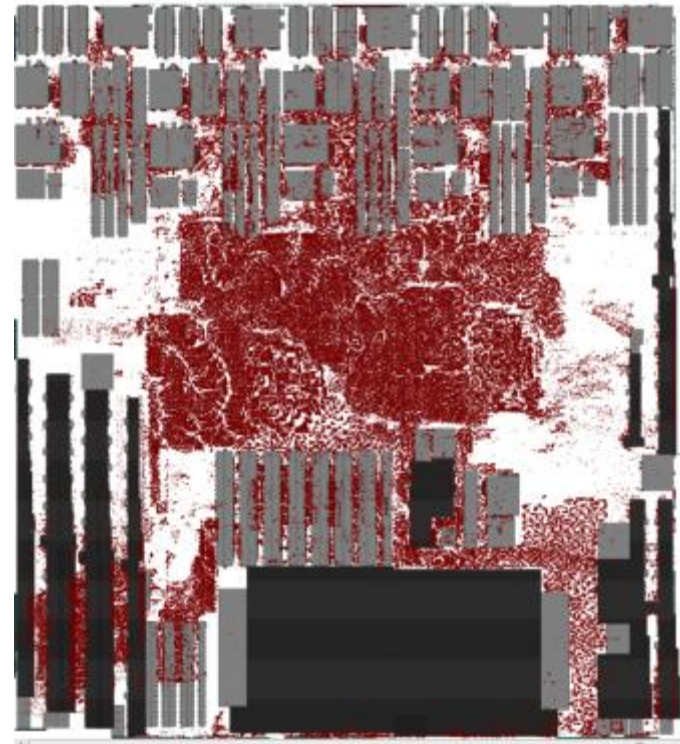
國際賽得獎榮譽 2023-2024

- Second Prize, ACM/IEEE ICCAD CAD Contest “Power and Timing Optimization Using Multibit Flip-Flop” (with Ho et al.), 2024
- Third Prize, ACM/IEEE ICCAD CAD Contest “Power and Timing Optimization Using Multibit Flip-Flop” (with Chen et al.), 2024
- First Prize, ACM/IEEE ICCAD CAD Contest “Static IR Drop Estimation Using Machine Learning” (with Liu et al.), 2023

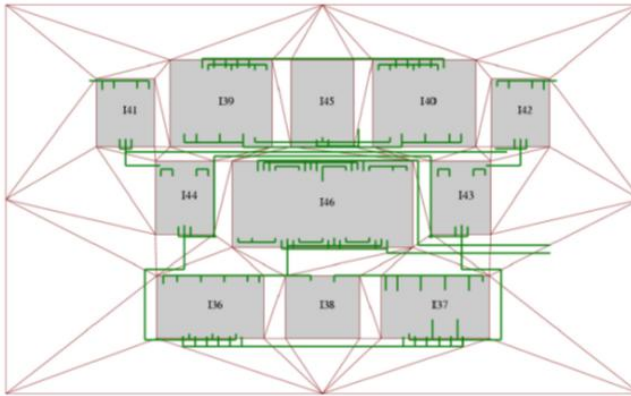


Award Winning Placer

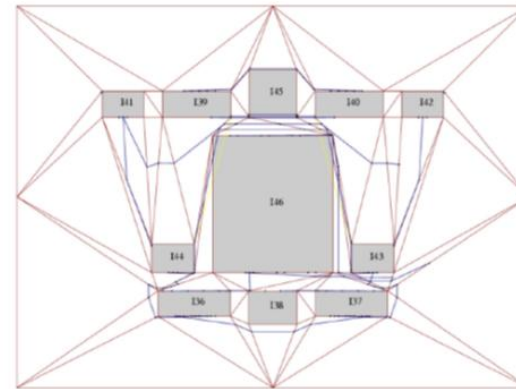
- ACM ISPD 2014 World Champion and 4th place FPGA placement contest
- Framework
 - SimPL based engine
 - Parallelized
- Applications
 - Thermal placement
 - FPGA heterogeneous routability-driven placement



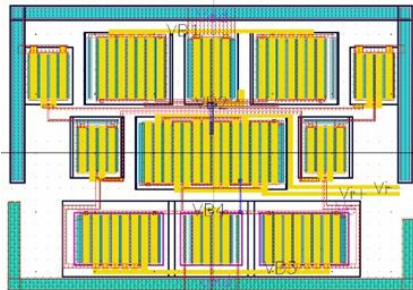
Analog Layout Migration and Generation



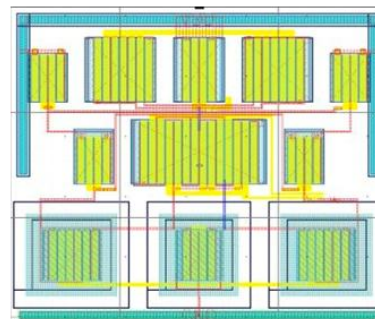
Original placement and routing with CDT extracted.(umc90)



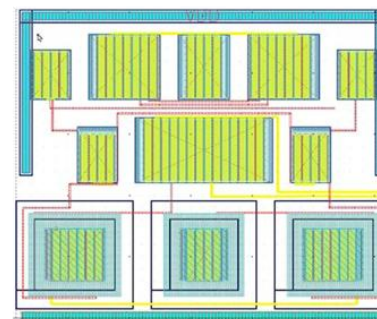
Target placement and recovered routing.(tsmc90)



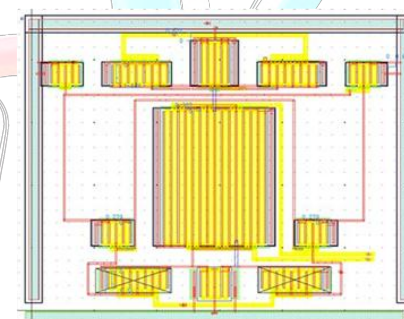
Opu90Manual



Opu65Manual



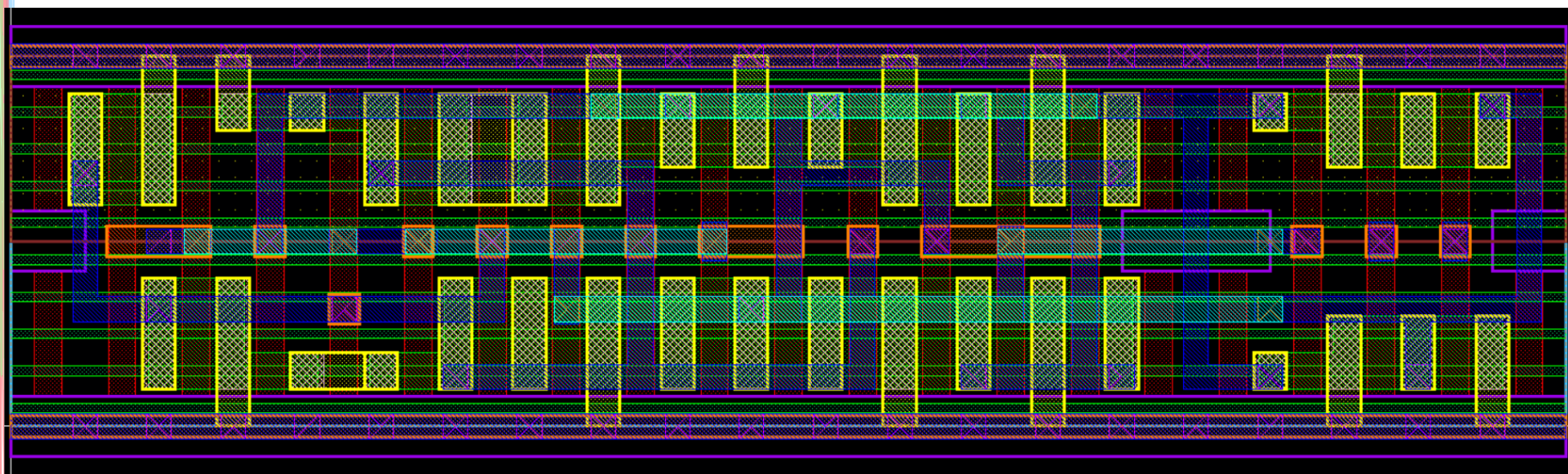
Opu65
Preserved



Opt90
Preserved

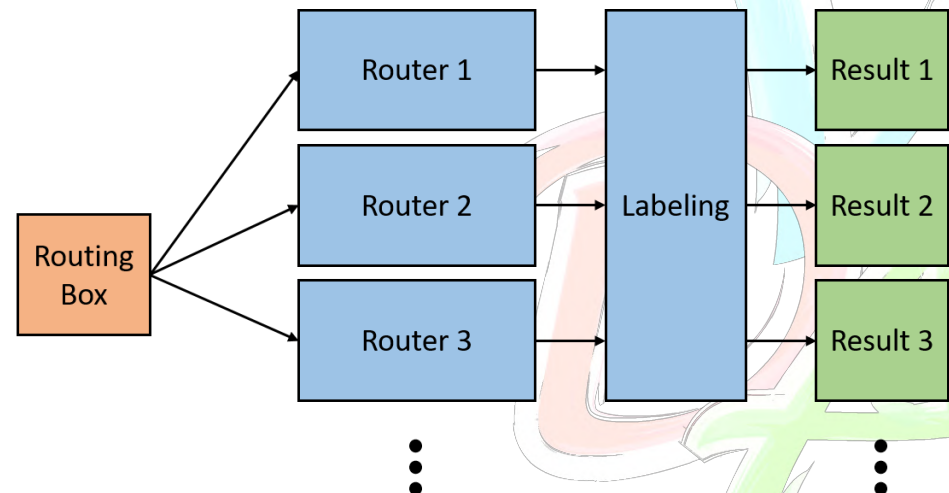
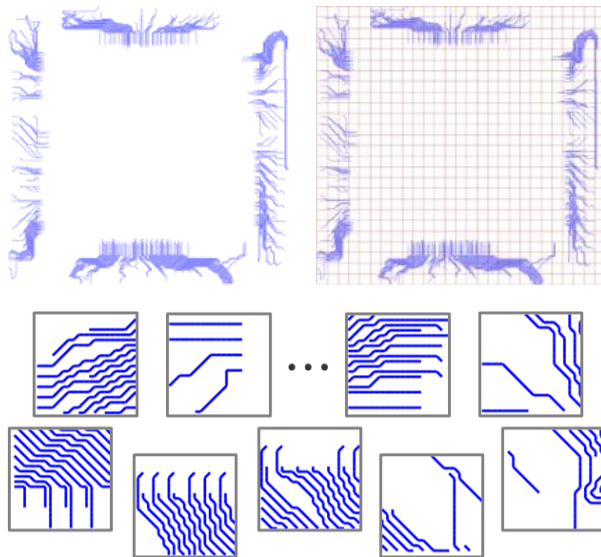
Advanced Cell Lib Generation

● ICGx3@ASAP7nm



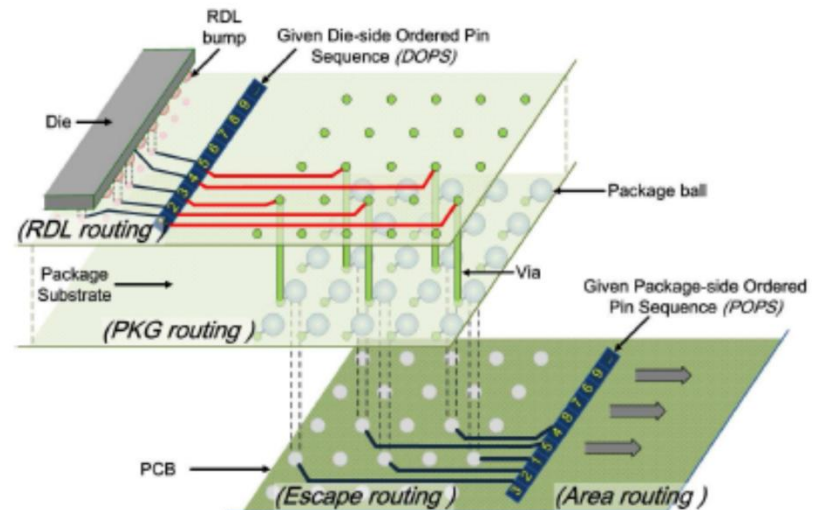
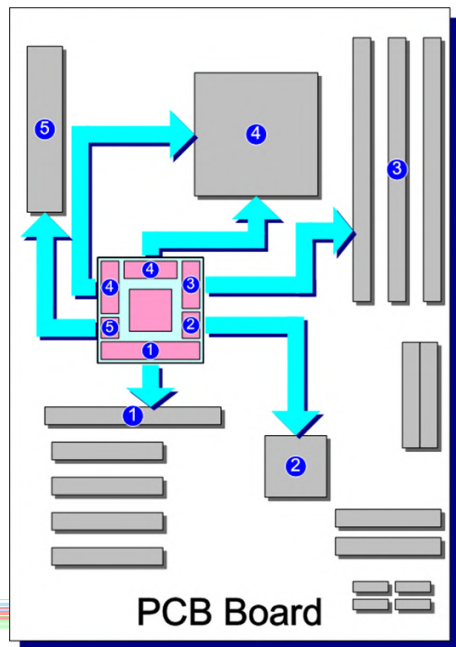
AI and ML/DL in EDA

- New methodologies from AI and machine learning
- Currently applied to noise sensor placement, routing/DRC violation prediction and IR-drop estimation
- Next steps include analog circuit design automation and package router



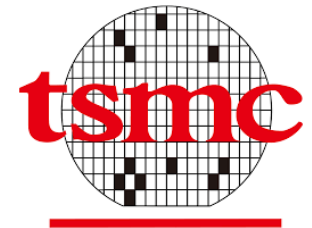
Chip/Package/Board Codesign

- 2.5D/3D integration power network synthesis and cosimulation
- Board aware pinout and board level routing
- Chip/Package decap insertion and optimization





Our Partners



People

- Current

- 5 PhD students (1 co-advised with Prof. Liu) + 18 master students

- Alumni

- Master: 100+
- PhD: 10+
- 畢業工作: 新思、益華(EDA)、TSMC (晶圓廠, EDA)、聯發科、聯詠、瑞昱 (IC設計)、創意 (IC設計服務)等



What Techniques Do We Need in EDA Business?

攻讀EDA需要甚麼技巧呢?

- The best of both worlds
- Software background
 - Algorithms and programming language
 - Data structures play important roles
- Hardware background
 - Device modeling
 - Interconnect modeling
 - Manufacture related issues
 - Circuit design and synthesis
- Combinatorial optimization
 - Unconstrained and constrained optimization
 - Mathematical programming
- Validation and verification techniques
 - Formal methods

歡迎加入我們!

- Prof. Hung-Ming Chen

- Office: ED 407

- TEL: 03-5731626

- hmchen@nycu.edu.tw

- <https://vdalab.web.nycu.edu.tw/advisor/>

- Lab (ED317B)

- <https://vdalab.web.nycu.edu.tw/>

- TEL:

- 03-5712121 (交大代表號)

- #54220

